

History of HPSDR Mercury and Quick Silver

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Early HPSDR and XYLO

In 2005 I started a High Performance SDR (HPSDR) project which was to consist of a motherboard carrying a FPGA/USB 2.0 interface and power supply with the provision for plug in modules through 40 pin headers. I had planned a narrow band high dynamic range module based on a QSD/DDS/PCM4202 audio ADC and a wide bandwidth module based on a high speed 16 bit ADC:

http://www.philcovington.com/SDR/PICS/HPSDR_FPGA_USB_Board_top1_800600.jpg

http://www.philcovington.com/SDR/PICS/HPSDR_FPGA_USB_Board_top4.jpg

I soon selected the LTC2208 ADC from Linear Technology. A representative from Linear Technology came across my blog (<http://pcovington.blogspot.com/>) and offered evaluation boards and samples to support the project.

At about the same time my HPSDR project came about, Phil Harman, VK6APH and Bill Tracey, KD5TFD were interested developing a sound card replacement to be used with the SDR-1000 and had started developing with a FPGA development board (XYLO) that had a high speed USB 2.0 interface. They formed the XYLO SDR group to support this. In March 2006, Phil Harman proposed that we merge my HPSDR project and XYLO SDR group into a common project since our goals were similar. By the middle of March 2006 an announcement was made that the groups would merge and the HPSDR.org website was set up.

HPSDR ATLAS and OZY

One of the first tasks was to define a backplane since various backplanes, such as passive PCI, were being proposed. I volunteered for the task which became the ATLAS backplane:

http://www.philcovington.com/HPSDR/ATLAS/REVA/atlas_1_REVA_BW.pdf

http://www.philcovington.com/HPSDR/ATLAS/ALPHA/Atlas_assy.pdf

We had an early volunteer to design an ATLAS plug-in FPGA/USB board to replace the XYLO board, but unfortunately the volunteer was not able to follow through with the task. I agreed to do the design for this board which became the HPSDR OZY board and to provide for the possibility of controlling a SDR-1000 through the OZY's IO ports that simulate a PC parallel port:

<http://www.philcovington.com/SDR/OZYREVA.jpg>

Early HPSDR Mercury

Soon after the OZY design was done I began to pursue Mercury. I initially used the Linear Technology supplied evaluation board for the LTC2208. In May of 2006 I became very busy with a work project so I

asked Phil Harman if he would like me to send him one of my LTC2208 evaluation boards to play with. I also sent Phil a Crystek low phase noise crystal oscillator that I had chosen as a candidate for driving the encode clock of the LTC2208 ADC. In the link below you can see the Mercury breadboard connected to the OZY. The LTC2208 evaluation board can be seen plugged in vertically to the breadboard with the RG 174/U cable running to the top of it:

http://hpsdr.org/wiki/index.php?title=Image:OZY_MERC_TEST.JPG

Quick Silver Version 1

In late 2006 I decided to design a board that I called Quick Silver (related to Mercury) which would become the initial prototype for HPSDR Mercury:

http://www.philcovington.com/SDR/PICS/QS1R_proto.JPG

http://www.philcovington.com/SDR/QS1RA_12012006.pdf

The initial thought about the design of HPSDR Mercury was that it would use either an Analog Devices AD6636 or AD6620 Digital Receive Signal Processor chip. The AD6636 was only available in BGA packaging so I chose to use two AD6620 DDCs on the Quick Silver (also called QS1R REV AB). I wanted to investigate whether the AD6620/6636 was suitable for use with the LTC2208 in a HF receiver and also to test the choice of low noise Crystek oscillator encode circuitry which would be critical in determining the LTC2208 ADC's performance.

It quickly became clear that the AD6620/6636 devices were not suitable from a dynamic range perspective for use in the HPSDR Mercury. About 90% of the DDC functionality was moved from the AD6620 into the Cyclone II FPGA on the QS1R REV AB prototype. There was not enough room in the FPGA to implement a useful final FIR compensating filter to correct for the passband droop of the CIC filters used in the FPGA implemented DDC. I then investigated using two external FIR filter chips made by a company called QuickFilter Technologies:

<http://www.quickfiltertech.com/files/QF1D512%20SavFIRe%20Datasheet.pdf>

Two of these chips were soon grafted on the QS1R board in place of the AD6620 parts for testing. These chips worked very well but I was concerned about their availability. I made a decision at that point to "bite the bullet" and wrote a one-tap-per-clock FIR filter in Verilog to move all of the DDC functionality into the FPGA. I was easily able to fit two 256 tap FIR filters into the remaining space in the Cyclone II FPGA which eliminated the need for the external QuickFilter FIR chips. During this time Altera also announced the availability of the Cyclone III FPGA in a QFP240 package with enough logical elements and hardware multipliers to be very interesting to SDR work – this also prompted me to develop the one-tap-per-clock FIR filter in Verilog since space would no longer be a concern with this FPGA.

The QS1R REV AB prototype allowed me to also test a Hittite HMC472 0-31.5 dB attenuator, a Sirenza SBF-4089/5089 RF Amp, Phil Harman's 1.5 MHz BPF stage, and a 30/60 MHz LPF stage that is planned to be used in the HPDR Mercury design.

The Quick Silver was the testing grounds for ideas that will be used in HPDR Mercury. Without experience gained from the QS1R REV AB prototype, we would have probably ended up with multiple alpha releases of the Mercury as we found these problems later.

Quick Silver QS1RT VERB

During the development and testing of the QS1R REV AB prototype, the Altera Cyclone III FPGA became available in a QFP240 package with enough logical elements to do some interesting SDR work. I wanted to investigate using a PCI or PCIe connection to the PC to allow much wider bandwidths to be processed than the USB 2.0 interface would allow. This is how QS1RT VERB came about. The VERB contains both the LTC2208 ADC and a TxDAC with a fiber optic or copper connection to a PCI/PCIe board in a PC. The high speed serial interface between the QS1RT and the PCI/PCIe card in the PC is made by a TI TLK2711 Serializer/Deserializer chip that transfers at 2.5 Gbps:

http://www.philcovington.com/SDR/PICS/QS1RT_VERB_MED.JPG

As of October 2007, I am in the process of testing the PCI end of the interface. This board uses some expensive components and is only really meant to be a demonstration of a high speed interface and for experimentation. I want to investigate the ultimate achievable bandwidth to the PC from the VERB and also configuration of the FPGA over the high speed fiber optic link.

Quick Silver QS1R REVB

Taking what I learned from QS1R REV AB prototype and QS1RT VERB, I set about designing a third (and hopefully final!) iteration of the Quick Silver board in October 2007. In previous boards, the RF section of the PCB was routed by hand and the digital sections were done by an auto router. In QS1R REVB, all routing was done by hand to optimize trace lengths and minimize vias in the digital sections of the circuit. The board was simplified with applications such as a HF receiver, VNA, spectrum analyzer, and digital oscilloscope in mind:

http://www.philcovington.com/SDR/qs1r_10112007.pdf

http://www.philcovington.com/SDR/qs1r_revb_sch.pdf

Included on the board is a 192 kSPS Stereo DAC for audio output. There are provisions to allow an expansion BPF/RF AMP/Attenuator board, an on-board 55 MHz LPF, a direct ADC input connector that bypasses the LPF, an I2C control bus, etc... See the schematic above for details.

The QS1R REV B PCB is completed, assembled, and now undergoing testing as of October 30, 2007.

